Specifications for the NI PXI-6541/6542

50/100 MHz Digital Waveform Generator/Analyzer

Typical values are representative of an average unit operating at room temperature. Specifications are subject to change without notice. For the most recent NI 6541/6542 specifications, visit `ni.com/manuals`.

To access the NI 6541/6542 documentation, including the *NI Digital Waveform Generator/Analyzer Getting Started Guide*, which contains functional descriptions of the NI 6541/6542 signals, navigate to **Start»Programs»National Instruments»NI-HSDIO»Documentation**.

Caution - Hot Surface Allow time to cool before extracting the NI 654*X* hardware from the PXI chassis to reduce risk of burns. Exercise caution when handling, as recently used NI 654*X* modules may exceed safe handling temperatures.

Contents

NATIONAL INSTRUMENTS

Channel Specifications

Specification	Value	Comments
Number of data channels	32	—
Direction control of data channels	Per channel	—
Number of Programmable Function Interface (PFI) channels	4	Refer to the *Waveform Specifications* section for more details.
Direction control of PFI channels	Per channel	—
Number of clock terminals	3 input 2 output	Refer to the *Timing Specifications* section for more details.

Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)

Specification	Value	Comments
Generation voltage families	1.8 V, 2.5 V, 3.3 V TTL (5 V TTL compatible)	Into 1 MΩ
Generation signal type	Single-ended	—

Specification	Value				Comments
Generation voltage levels	Low Voltage Levels		High Voltage Levels		—
	Typical	Maximum	Minimum	Typical	
1.8 V	0 V	0.1 V	1.7 V	1.8 V	I = 100 µA
2.5 V	0 V	0.1 V	2.4 V	2.5 V	
3.3 V	0 V	0.1 V	3.2 V	3.3 V	
5.0 V	0 V	0.1 V	3.2 V	3.3 V	
Output impedance	50 Ω nominal				—
Maximum DC drive strength	±8 mA at 1.8 V ±16 mA at 2.5 V ±32 mA at 3.3 V				—
Data channel driver enable/disable control	Per channel				Software-selectable
Channel power-up state	Drivers disabled, 10 kΩ input impedance				—
Output protection	The device can indefinitely sustain a short to any voltage between 0 V and 5 V.				—

Acquisition Channels (Data, STROBE, and PFI <0..3>)

Specification	Value		Comments
Acquisition voltage families	1.8 V, 2.5 V, 3.3 V TTL (5 V TTL compatible)		—
Acquisition voltage levels	Low Voltage Threshold	High Voltage Threshold	—
	Maximum	Minimum	
1.8 V	0.45 V	1.35 V	—
2.5 V	0.75 V	1.75 V	—
3.3 V	1.00 V	2.30 V	—
5.0 V	1.00 V	2.30 V	—

Specification	Value	Comments
Input impedance	High-impedance (10 kΩ)	—
Input protection	–1 V to 6 V	Diode clamps in the design may provide additional protection outside this range.

Timing Specifications

Sample Clock

Specification	Value	Comments
Sample clock sources	1. On Board Clock (internal voltage-controlled crystal oscillator (VCXO) with divider) 2. CLK IN (SMB jack connector) 3. PXI_STAR (PXI backplane) 4. STROBE (DDC connector; acquisition only)	—
On Board Clock frequency range	**NI 6541**: 48 Hz to 50 MHz Configurable to 200 MHz/N; $4 \le N \le 4{,}194{,}304$ **NI 6542**: 48 Hz to 100 MHz Configurable to 200 MHz/N; $2 \le N \le 4{,}194{,}304$	—
CLK IN frequency range	**NI 6541**: 20 kHz to 50 MHz **NI 6542**: 20 kHz to 100 MHz	Refer to the *CLK IN (SMB Jack Connector)* section for restrictions based on waveform type.
PXI_STAR frequency range	**NI 6541**: 48 Hz to 50 MHz **NI 6542**: 48 Hz to 100 MHz	Refer to the *PXI_STAR (PXI Backplane)* section.

Specification	Value		Comments
STROBE frequency range	**NI 6541**: 48 Hz to 50 MHz **NI 6542**: 48 Hz to 100 MHz		Refer to the *STROBE (Digital Data & Control (DDC) Connector)* section.
Sample clock relative delay adjustment range	0 to 1 Sample clock period		You can apply a delay or phase adjustment to the On Board Clock to align multiple devices.
Sample clock relative delay adjustment resolution	10 ps		
Exported Sample clock destinations	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMB jack connector)		Sample clocks with sources other than STROBE can be exported.
Exported Sample clock delay range (δ_C)	0 to 1 Sample clock periods		For clock frequencies ≥25 MHz
Exported Sample clock delay resolution (δ_C)	1/256 of Sample clock period		For clock frequencies ≥25 MHz
Exported Sample clock jitter	**Period Jitter**	**Cycle-to-Cycle Jitter**	Typical; using On Board Clock
	20 ps_{rms}	35 ps_{rms}	

Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)

Specification	Value	Comments
Data channel-to-channel skew	±600 ps	Typical skew across all data channels
Maximum data channel toggle rate	**NI 6541**: 25 MHz **NI 6542**: 50 MHz	—
Data position modes	Rising edge, Falling edge, or Delayed	Relative to Sample clock
Generation data delay range (δ_G)	0 to 1 Sample clock period	For clock frequencies ≥25 MHz
Generation data delay resolution (δ_G)	1/256 of Sample clock period	For clock frequencies ≥25 MHz
Exported Sample clock offset (t_{CO})	0 ns or 2.5 ns (default)	Software-selectable
Time delay from Sample clock (internal) to DDC connector (t_{SCDDC})	8.4 ns	Typical

Generation Provided Setup and Hold Times

Exported Sample Clock Mode and Offset	Voltage Family	Time from Rising Clock Edge to Data Transition (t_{PCO})	Minimum Provided Setup Time (t_{PSU})	Minimum Provided Hold Time (t_{PH})
Noninverted, 2.5 ns	1.8V	2.5 ns typical	t_P – 5.5 ns	0.5 ns
	2.5V		t_P – 4.5 ns	0.9 ns
	3.3V		t_P – 4 ns	1 ns
	5.0V		t_P – 4 ns	1 ns
Inverted, 0 ns	1.8V	$t_P/2$	$t_P/2$ – 3.5 ns	$t_P/2$ – 1.5ns
	2.5V		$t_P/2$ – 2.5 ns	
	3.3V		$t_P/2$ – 2 ns	
	5.0V		$t_P/2$ – 2 ns	

To determine the appropriate exported Sample clock mode and offset for your NI 654*X* generation session, compare the setup and hold times from the datasheet of your device under test (DUT) to the values in this table. Select the Exported Sample Clock mode and offset such that the NI 654*X* provided setup and hold times are greater than the setup and hold times required for the DUT.

Refer to Figure 1 for a diagram illustrating the relationship between the exported Sample clock mode and the provided setup and hold times.

Note: This table assumes the Data Position is set to the rising edge of the Sample Clock and the Sample Clock is exported to the DDC connector.

Note: This table includes worst-case effects of channel-to-channel skew, inter-symbol interference, and jitter.

Note: Other combinations of Exported Sample Clock mode and offset are also allowed. The preceding table only presents the values for the default case (noninverted clock with 2.5 ns offset) and the case for providing balanced setup and hold times (inverted clock with 0 ns offset).

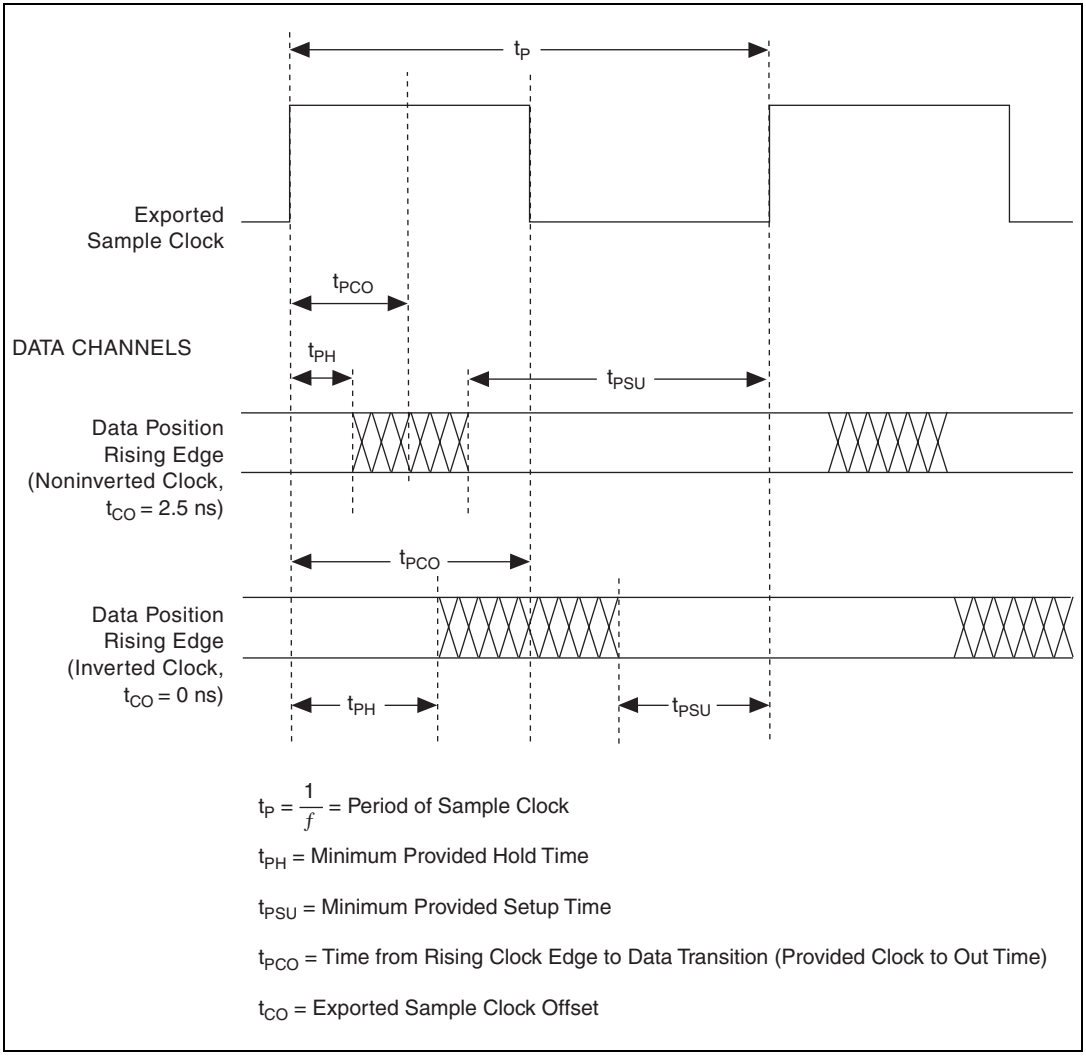
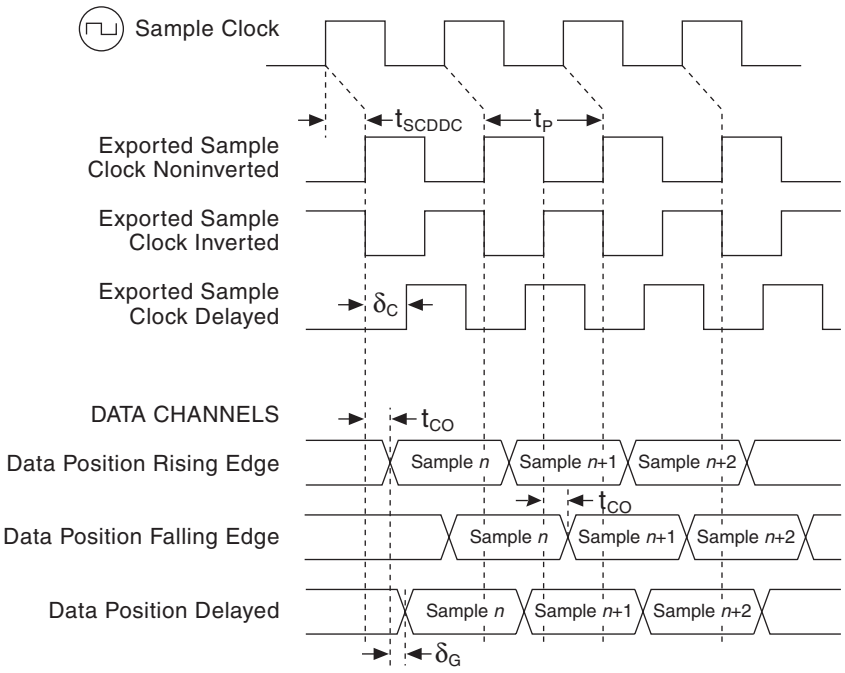


Figure 1. Generation Provided Setup and Hold Times Timing Diagram



t_{SCDDC} : Time delay from Sample Clock (internal) to DDC Connector

$0 \leq \delta_C \leq 1$: Exported Sample Clock Delay (fraction of t_P)

$0 \leq \delta_G \leq 1$: Pattern Generation Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{CO} = Exported Sample Clock Offset; 0 or 2.5 ns, software-selectable

Figure 2. Generation Timing Diagram

Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)

Specification	Value	Comments
Channel-to-channel skew	±600 ps	Typical skew across all data channels
Set-up time to STROBE (t_{SUS})	3.1 ns	Maximum; includes maximum data channel-to-channel skew
Hold time to STROBE (t_{HS})	2.7 ns	Maximum; includes maximum data channel-to-channel skew
Time delay from DDC connector to internal Sample clock (t_{DDCSC})	14.4 ns	Typical
Set-up time to Sample clock (t_{SUSC})	0.4 ns	Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}
Hold time to Sample clock (t_{HSC})	0 ns	Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}
Acquisition data delay range (δ_A)	0 to 1 Sample clock periods	For clock frequencies ≥25 MHz
Acquisition data delay resolution (δ_A)	1/256 of Sample clock period	For clock frequencies ≥25 MHz

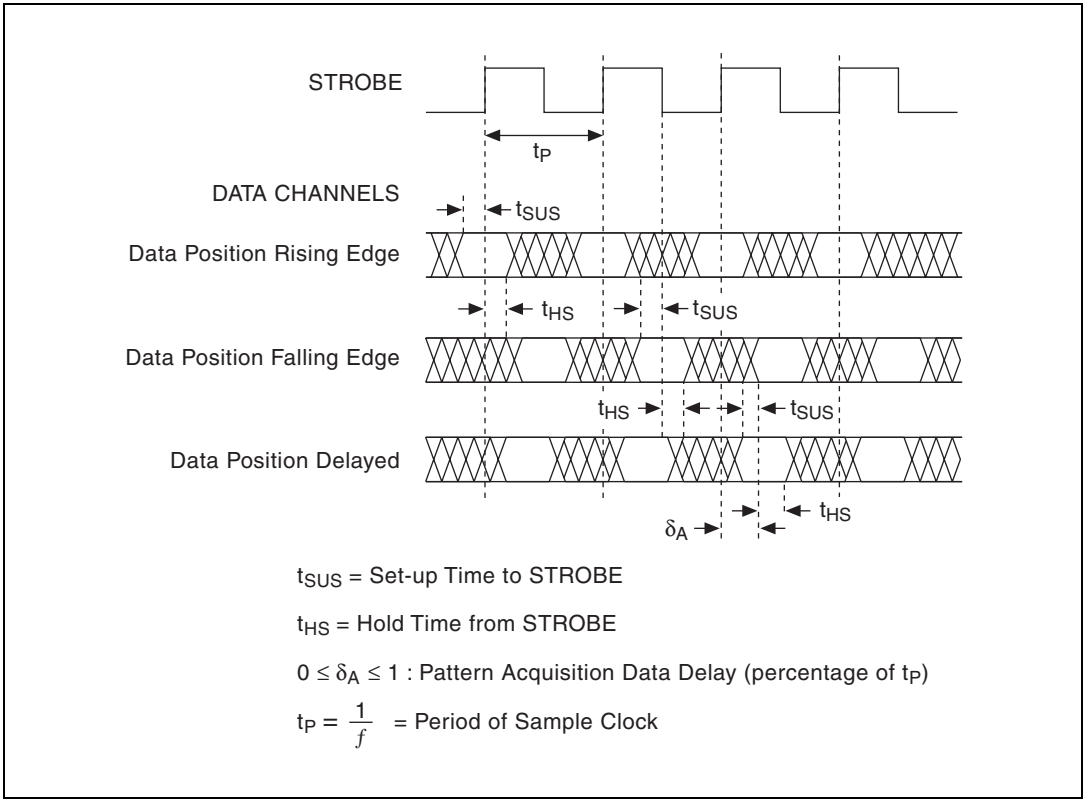
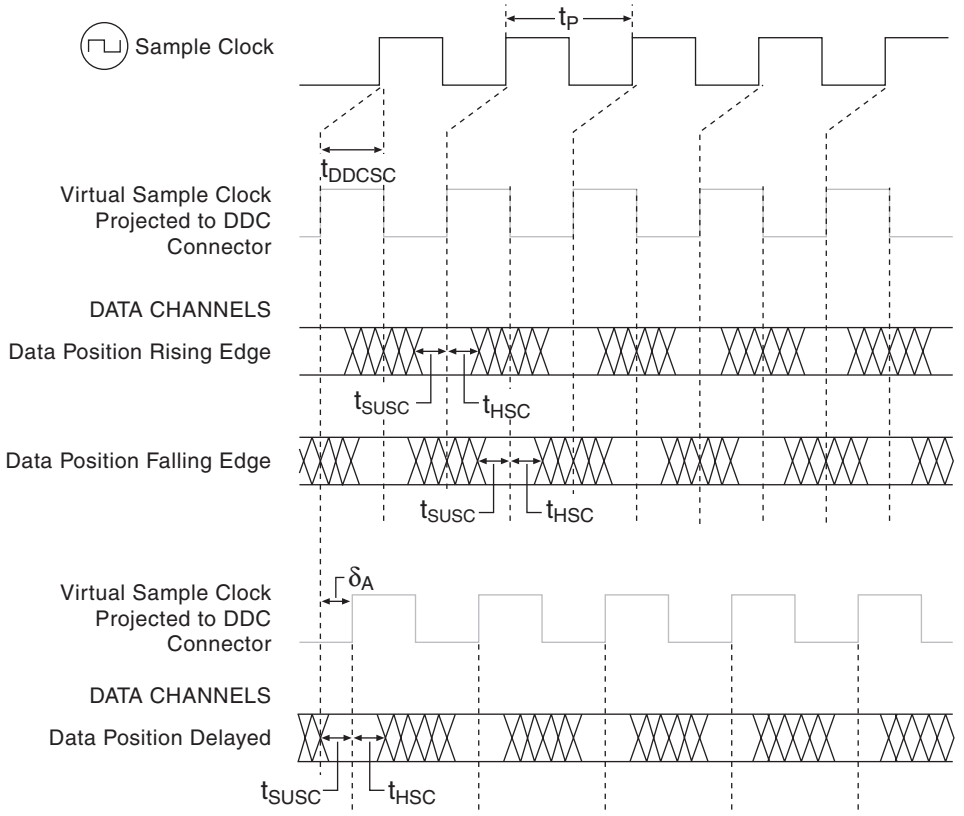


Figure 3. Acquisition Timing Diagram Using STROBE as the Sample Clock



t_{DDCSC} : Time Delay from DDC Connector to Internal Sample Clock

$0 \leq \delta_A \leq 1$: Pattern Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

Figure 4. Acquisition Timing Diagram with Sample Clock Sources Other than STROBE

CLK IN (SMB Jack Connector)

Specification	Value				Comments
Direction	Input into device				—
Destinations	1. Reference clock (for the phase lock loop (PLL)) 2. Sample clock				—
Input coupling	AC				—
Input protection	±10 VDC				—
Input impedance	50 Ω (default) or 1 kΩ				Software-selectable
Minimum detectable pulse width	4 ns				Required at V_{rms} mean
Clock requirements	Clock must be continuous and free-running				—
As Sample clock					
External Sample clock range	**Square Waves**				—
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}			—
	Frequency range	**NI 6541**: 20 kHz to 50 MHz			—
		NI 6542: 20 kHz to 100 MHz			—
	Duty cycle range	f < 50 MHz: 25% to 75% f ≥ 50 MHz: 40% to 60%			—
	Sine Waves				—
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}	1.0 V_{pp} to 5.0 V_{pp}	2.0 V_{pp} to 5.0 V_{pp}	—
	Frequency range	**NI 6541**: 5.5 MHz to 50 MHz	**NI 6541**: 3.5 MHz to 50 MHz	**NI 6541**: 1.8 MHz to 50 MHz	—
		NI 6542: 5.5 MHz to 100 MHz	**NI 6542**: 3.5 MHz to 100 MHz	**NI 6542**: 1.8 MHz to 100 MHz	—

Specification	Value	Comments
As Reference Clock		
Reference clock frequency range	10 MHz ±50 ppm	—
Reference clock voltage range	0.65 V_{pp} to 5.0 V_{pp}	—
Reference clock duty cycle	25% to 75%	—

STROBE (Digital Data & Control (DDC) Connector)

Specification	Value	Comments
Direction	Input into device	—
Destinations	Sample clock (acquisition only)	—
STROBE frequency range	**NI 6541**: 48 Hz to 50 MHz **NI 6542**: 48 Hz to 100 MHz	—
STROBE duty cycle range	**NI 6541**: 25%–75% for clock frequencies <50 MHz **NI 6542**: 40%–60% for clock frequencies ≥50 MHz 25%–75% for clock frequencies <50 MHz	At the programmed threshold
Minimum detectable pulse width	4 ns	Required at both acquisition voltage thresholds
Voltage thresholds	Refer to the *Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)* specifications in the *Channel Specifications* section.	—
Clock requirements	Clock must be continuous and free-running	—
Input impedance	10 kΩ	—

PXI_STAR (PXI Backplane)

Specification	Value	Comments
Direction	Input into device	—
Destinations	1. Sample clock 2. Start trigger 3. Pause trigger (generation sessions only) 4. Script trigger <0..3> (generation sessions only) 5. Reference trigger (acquisition sessions only)	—
PXI_STAR frequency range	**NI 6541**: 48 Hz to 50 MHz **NI 6542**: 48 Hz to 100 MHz	—
Clock requirements	Clock must be continuous and free-running	—

CLK OUT (SMB Jack Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)	—
Output impedance	50 Ω nominal	—
Electrical characteristics	Refer to the *Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)* specifications in the *Channel Specifications* section.	—
Maximum drive current	8 mA at 1.8V, 16 mA at 2.5V, 32 mA at 3.3V	—
Logic type	Generation logic family setting (3.3V, 2.5V, 1.8V)	—

DDC CLK OUT (Digital Data & Control (DDC) Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	Sample clock	STROBE cannot be routed to DDC CLK OUT
Electrical characteristics	Refer to the *Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)* specifications in the *Channel Specifications* section.	—

Reference Clock (PLL)

Specification	Value	Comments
Reference clock sources	1. PXI_CLK10 (PXI backplane) 2. CLK IN (SMB jack connector) 3. None (internal oscillator not locked to a reference)	Provides the reference frequency for the phase lock loop
Lock time	400 ms	Typical
Reference clock frequencies	10 MHz ±50 ppm	—
Reference clock duty cycle range	25% to 75%	—
Reference clock destinations	CLK OUT (SMB jack connector)	—

Waveform Specifications

Memory and Scripting

Specification	Value			Comments
Memory architecture	The NI 654*X* uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user-defined.			Refer to the *Onboard Memory* section in the *NI Digital Waveform Generator/ Analyzer Help* for more information.
Onboard memory size	1 Mbit/channel (for generation sessions) 1 Mbit/channel (for acquisition sessions)	8 Mbit/channel (for generation sessions) 8 Mbit/channel (for acquisition sessions)	64 Mbit/channel (for generation sessions) 64 Mbit/channel (for acquisition sessions)	Maximum limit for generation sessions assumes no scripting instructions.
Generation modes	**Single-waveform mode**: Generate a single waveform once, *n* times, or continuously.			—
	Scripted mode: Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.			

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td rowspan="5">Generation minimum waveform size (Samples)</td><td rowspan="2">Configuration</td><td colspan="2">Sample Rate</td><td rowspan="5">Sample rate dependent. Increasing sample rate increases minimum waveform size requirement.
For information on these configurations, refer to Common Scripting Use Cases in the NI Digital Waveform Generator/ Analyzer Help.</td></tr>
<tr><td>100 MHz (NI 6542 only)</td><td>50 MHz</td></tr>
<tr><td>Single waveform</td><td>2</td><td>2</td></tr>
<tr><td>Continuous waveform</td><td>32</td><td>16</td></tr>
<tr><td>Stepped sequence</td><td>128</td><td>64</td></tr>
<tr><td></td><td>Burst sequence</td><td>512</td><td>256</td></tr>
<tr><td>Generation finite repeat count</td><td colspan="3">1 to 16,777,216</td><td>—</td></tr>
<tr><td>Generation waveform quantum</td><td colspan="3">Waveform size must be an integer multiple of two samples.</td><td>Regardless of waveform size, NI-HSDIO allocates waveforms into block sizes of 32 S of physical memory.</td></tr>
<tr><td>Acquisition minimum record size</td><td colspan="3">1 sample</td><td>Regardless of waveform size, NI-HSDIO allocates at least 128 bytes for a record.</td></tr>
<tr><td>Acquisition record quantum</td><td colspan="3">1 sample</td><td>—</td></tr>
</table>

Specification	Value	Comments
Acquisition maximum number of records	1 record	—
Acquisition number of pre-Reference trigger samples	0 up to full record	—
Acquisition number of post-Reference trigger samples	0 up to full record	—

Triggers (Inputs to the NI 654*X*)

Specification	Values	Comments
Trigger types	1. Start trigger 2. Pause trigger 3. Script trigger <0..3> (generation sessions only) 4. Reference trigger (acquisition sessions only)	—
Sources	1. PFI 0 (SMB jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane) 4. PXI_STAR (PXI backplane) 5. Pattern match (acquisition sessions only) 6. Software (user function call) 7. Disabled (do not wait for a trigger)	—
Trigger detection	1. Start trigger (edge detection: rising or falling) 2. Pause trigger (level detection: high or low) 3. Script trigger <0..3> (edge detection: rising or falling; level detection: high or low) 4. Reference trigger (edge detection: rising or falling)	—

<table>
<tr><th>Specification</th><th colspan="2">Values</th><th>Comments</th></tr>
<tr><td>Minimum required trigger pulse width</td><td colspan="2">40 ns</td><td></td></tr>
<tr><td>Destinations</td><td colspan="2">1. PFI 0 (SMB jack connectors)
2. PFI <1..3> (DDC connector)
3. PXI_TRIG<0..7> (PXI backplane)</td><td>Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported.</td></tr>
<tr><td rowspan="2">Delay from Pause trigger to Pause state</td><td>Generation Sessions</td><td>Acquisition Sessions</td><td>—</td></tr>
<tr><td>32 Sample clock periods + 150 ns</td><td>Synchronous with the data</td><td>Use the Data Active event during generation to determine when the NI 654X enters the Pause state.</td></tr>
<tr><td>Delay from trigger to digital data output</td><td colspan="2">32 Sample clock periods + 160 ns</td><td>—</td></tr>
</table>

Events (Generated from the NI 654*X*)

Specification	Value	Comments
Event type	1. Marker <0..3> (generation sessions only) 2. Data Active event (generation sessions only) 3. Ready for Start event	—
Destinations	1. PFI 0 (SMB jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane)	Each event can be routed to any destination, except the Data Active event. The Data Active event can only be routed to the PFI channels.
Marker time resolution (placement)	Markers must be placed at an integer multiple of two samples.	—

Miscellaneous

Specification	Value	Comments
Warm-up time	15 minutes	—
On Board Clock characteristics (valid when PLL reference source is set to None)		
Frequency accuracy	±100 ppm	Typical
Temperature stability	±30 ppm	Typical
Aging	±5 ppm first year	Typical

Power

Specification	Value		Comments
	Typical	Maximum	—
+3.3 VDC	1.6 A	1.8 A	—
+5 VDC	1.2 A	1.7 A	—
+12 VDC	0.25 A	0.40 A	—
–12 VDC	0.06 A	0.10 A	—
Total power	15 W	20.5 W	—

Software

Specification	Value	Comments
Driver software	NI-HSDIO driver software 1.2 or later. NI-HSDIO allows you to configure and control the NI 654*X*. NI-HSDIO provides application interfaces for many development environments. NI-HSDIO follows IVI API guidelines.	—
Application software	NI-HSDIO provides programming interfaces for the following application development environments: • National Instruments LabVIEW 7.0 or later • National Instruments LabWindows™/CVI™ 6.0 or later • Microsoft Visual C/C++ 6.0 or later	—
Test panel	National Instruments Measurement & Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 654*X*. MAX is included on the NI-HSDIO driver CD.	—

Environment

Note To ensure that the NI 654*X* cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included with the NI 654*X*. The NI 654*X* is intended for indoor use only.

Specification	Value	Comments
Operating temperature	0 ºC to +55 ºC in all NI PXI chassis except the following: 0 ºC to +45 ºC when installed in an NI PXI-1000/B and NI PXI-101*X* chassis (Meets IEC-60068-2-1 and IEC-60068-2-2.)	—
Storage temperature	–20 °C to 70 °C	—
Operating relative humidity	10% to 90% relative humidity, noncondensing (Meets IEC-60068-2-56)	—
Storage relative humidity	5% to 95% relative humidity, noncondensing (Meets IEC-60068-2-56)	—
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Storage shock	50 g, half-size, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (Meets IEC-60068-2-64.)	—
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.)	—
Altitude	0 m to 2,000 m above sea level (at 25 ºC ambient temperature)	—
Pollution Degree	2	—

Safety, Electromagnetic Compatibility, and CE Compliance

Safety	The NI 654*X* meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use: • IEC 61010-1, EN 61010-1 • UL 61010-1 • CAN/CSA C22.2 No. 61010-1	For UL and other safety certifications, refer to the product label or to `ni.com`.
Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	—
Immunity	EN 61326:1997 + A2:2001, Table 1	—
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant.	—
This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:		
Low-Voltage Directive (safety)	73/23/EEC	—
Electro-magnetic Compatibility Directive (EMC)	89/336/EEC	—
For EMC compliance, operate this device with shielded cabling. In addition, filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.		

Physical Specifications

Specification	Value		Comments
Dimensions	18.6 cm × 13.1 cm (7.32 in. × 5.16 in.) Single 3U CompactPCI slot; PXI compatible		—
Weight	343.03 g (12.1 oz.)		—
Front Panel Connectors			
Label	**Function(s)**	**Connector Type**	—
CLK IN	External Sample clock, external PLL reference input	SMB jack connector	—
PFI 0	Events, triggers	SMB jack connector	—
CLK OUT	Exported Sample clock, exported Reference clock	SMB jack connector	—
DIGITAL DATA & CONTROL	Digital data channels, exported Sample clock, STROBE, events, triggers	68-pin VHDCI connector	—

373771A-01 Jul04